



# Computer Memory Test Labs

## Intel® Approved Final Test Report

MOTHERBOARD	MANUFACTURER	CHIPSET	TEST #	STATUS
NUC7i7BNH	Intel	Intel® Kaby Lake	027120	PASSED

### MEMORY MODULE INFORMATION

**CMTL Part #: GSL026**

Manufacturer Name: **G.SKILL**

Manufacturer Part #: **F4-2133C15D-16GRS (Kit size: 8GBx2)**

DRAM Manufacturer: **Skhynix**

Environment Code: **RoHS**

DRAM Part #: **H5AN4G8NAFR-TFC**

Low Profile: **30mm LP**

Module Config: **1024M x 64**

Cas Latency: **15**

Module Size: **8GB**

Bank: **2**

PCB Part #: **BA4SRCE1 0.51**

PCB Layer Count: **10 Layer** Assembly Type: **JEDEC Standard**

Module Information: **Unbuffered 1.2V    Non-ECC    2133MHz    DDR4 SODIMM**

SYSTEM INFORMATION	TESTING DETAILS
<p><b><u>MINIMUM SYSTEM INFORMATION</u></b></p> <p>Minimum System: NUC7i7BNH            Serial Number: GEBN711005H8            Board Revision: J31145-302            Bios Memory Count: 8GB            Processor Code: Intel® Core™ i7-7567U @ 3.50GHz            Bios at time of test: BNKBL357.86A.0042.2017.0303.1854            RST PRO Count: 9G 1008M</p> <p><b><u>MAXIMUM SYSTEM INFORMATION</u></b></p> <p>Maximum System: NUC7i7BNH            Serial Number: GEBN711005TP            Board Revision: J31145-302            Bios Memory Count: 16GB            Processor Code: Intel® Core™ i7-7567U @ 3.50GHz            Bios at time of test: BNKBL357.86A.0042.2017.0303.1854            R.S.T PRO Count: 17G 1008M</p>	<p><b>35°C~55°C Temperature / Standard Voltage</b></p> <p>Start Date: 5/26/2017            Stop Date: 5/27/2017            Insertion Test: Pass            SPD Check: Pass            Minimum Load: Pass            Maximum Load: Pass            S0 ~ S5 Test: Pass            Power Cycle Test: Pass            Test Card Version: R.S.T Premium v8.50</p>

Microsoft Windows-7 64bit version is used as it support over 4GB memory and must support target chipset/CPU platform. All board drivers must be loaded when drivers are available on Intel web site. Front panel power cycling test, ACPI S3 sleep state cycling test, and Hibernate S4/S5 state cycling test is done up to 20 cycle each when the board support it. At least 2 loops of all test under R.S.T PRO3 to be completed.

**Test Notes:**

Min configuration, 5 Loops Passed, 0 Error; Memory speed running @ 2133MHz  
 Max configuration, 5 Loops Passed, 0 Error; Memory speed running @ 2133MHz  
 UUT under test reached +35°C